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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,996	10/30/2003	Takashi Miyamori	244612US2CONT	5652

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ALEXANDRIA, VA 22314

EXAMINER

KIM, KENNETH S

ART UNIT PAPER NUMBER

2111

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/695,996

Applicant(s)

MIYAMORI, TAKASHI

Examiner

Kenneth S KIM

Art Unit

2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 30 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 21-50 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 21-50 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

KENNETH S. KIM  
PRIMARY EXAMINER

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☒ Certified copies of the priority documents have been received in Application No. 09/604,907.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 10/30/2003.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

1. Claims 21-50 are presented for examination.
2. Applicant is reminded that there is a typographical error in the citation of the related application serial number in the preliminary amendment to the specification.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 29 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 29, "the operation mode register" lacks antecedent basis.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 21, 22, 24, 26-40, 42, and 44-50 are rejected under 35 U.S.C. 102(e) as being anticipated by Levy, U.S. Patent No. 5,923,892.

Levy teaches the invention as claimed in claim 21 including a parallel processor for processing a plurality of operation instructions in one cycle in parallel including:

- (a) a first operation processor (22, host processor),
- (b) at least one second operation processor (38, coprocessor),
- (c) the first operation processor including, a control unit for, in case that an operation mode indicating whether or not the second operation processor should be run in parallel (col. 10, line 52) to carry out an operation instruction is a first operation mode (halt mode; col. 8, line 44), in accordance with the operation mode, supplying the first operation processor with an instruction sequence that defines an operation of the first operation processor, and for generating a control signal to halt an operation of the second operation processor and supplying the control signal to the second operation processor (col. 8, line 55),
- (d) an instruction execution unit for switching the operation mode in accordance with an input decoded instruction (col. 8, line 58),
- (e) wherein the operation mode has a first operation mode in which the first operation processor alone is operated, and a second instruction mode in which both of the first operation processor and the second operation processor are operated (col. 8, line 44; coprocessor is in halt or run mode), and

further teaches as in claims 22, 24, and 26-38,

- (f) wherein in case that the operation mode is the second operation mode, the control unit supplies the first operation processor with an instruction string that defines an operation of the first operation processor, and supplies the second operation processor

with an instruction string that defines an operation of the second operation processor (col. 10, line 52) – claims 22 and 24,

(g) wherein the control signal is a signal that stops a supply of a clock or a disable signal (methods of halting) – claims 26 and 27,

(h) wherein a subroutine call instruction to switch operation mode is executed (col. 8, line 58) by inverting the value of operation mode in a register (col. 8, line 56) – claims 28-31,

(i) wherein the value of operation mode is determined by a jump address (portions of program instructions that require the coprocessor is identified by a jump address to that portion) – claim 32

(j) wherein a plurality of coprocessor are individually controlled for parallel processing such as for processing an SIMD instruction (duplication of the control of a coprocessor) – claims 33-35, and

(k) selecting instructions in an instruction register of a first and second portion for supplying the first operation processor (instructions in a dual width register are alternatively supplied to a processor) – claims 36-38.

The system claims 39, 40, 42, and 44-48, the method claim 49, and the processor claim 50 are equivalently rejected based on the same reason.

7. Claims 21-27 and 32-50 are rejected under 35 U.S.C. 102(e) as being anticipated by Boutaud et al, U.S. Patent No. 5,838,934.

Boutaud et al teaches the invention as claimed in claim 21 including a parallel processor for processing a plurality of operation instructions in one cycle in parallel including:

- (a) a first operation processor (400, host processor),
- (b) at least one second operation processor (300, processor),
- (c) the first operation processor (col. 1, line 26) including, a control unit for, in case that an operation mode (col. 16, line 13) indicating whether or not the second operation processor should be run in parallel (col. 16, line 15) to carry out an operation instruction is a first operation mode (HOM mode; col. 13, line 38), in accordance with the operation mode, supplying the first operation processor with an instruction sequence that defines an operation of the first operation processor, and for generating a control signal to halt an operation of the second operation processor and supplying the control signal to the second operation processor (col. 13, line 40),
- (d) an instruction execution unit for switching the operation mode in accordance with an input decoded instruction (host can control upon decoding an instruction),
- (e) wherein the operation mode has a first operation mode in which the first operation processor alone is operated, and a second instruction mode in which both of the first operation processor and the second operation processor are operated (col. 16, line 13; processor is in stopped or run mode), and

further teaches as in claims 22-27 and 32-38,

- (f) wherein in case that the operation mode is the second operation mode, the control unit supplies the first operation processor with an instruction string that defines an

operation of the first operation processor, and supplies the second operation processor with an instruction string that defines an operation of the second operation processor (col. 16, line 15) – claims 22 and 24,

(g) supplying NOP retained in a memory to the second operation processor (col. 13, line 62) – claims 23 and 25,

(h) wherein the control signal is a signal that stops a supply of a clock or a disable signal (col. 13, line 40) – claims 26 and 27,

(i) wherein the value of operation mode is determined by the jump address (portions of program instructions that require the coprocessor is identified by a jump address to that portion) – claim 32

(j) wherein a plurality of coprocessor are individually controlled for parallel processing such as for processing SIMD instruction (duplication of the control of a coprocessor) – claims 33-35, and

(k) selecting instructions in a instruction register of a first and second portion for supplying the first operation processor (instructions in a dual width registers are alternatively supplied to a processor) – claims 36-38.

The system claims 39-48, the method claim 49, and the processor claim 50 are equivalently rejected based on the same reason.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Watanabe et al taught a method of selectively deactivating processors executing in SIMD and MIMD modes using NOP instruction.

MacDonald taught a method of disabling a processor by disabling clock signal.

Applicant is reminded of the features taught in the reference submitted by the applicant.

Tan et al taught a method of selectively supplying instructions from dual width register and operation mode determined by jump address.

Debnath et al taught a method of disabling floating-point processor.

Kohn taught a method of switching between dual instruction mode and single instruction mode based on decoded instruction bit signal.

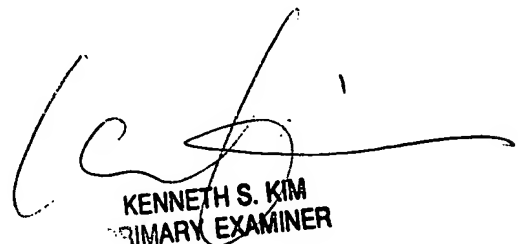
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth S KIM whose telephone number is (571) 272-3627. The examiner can normally be reached on M-F (8:30-17:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

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February 2, 2005



KENNETH S. KIM  
PRIMARY EXAMINER